Perfluorocompounds Emissions Reduction in the Semiconductor and Silicon Industries

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The environmental impact of a typical semiconductor Fab
(30,000 wafer starts / month)

- **Si wafers**
  - 10 tons/yr

- **Electricity**
  - 0.9kWh/cm² of Si produced
  - ~ a town of 7,500.

- **Air emissions**
  - HAPs (max 20 tons/yr)
  - VOCs (max 40-100 tons/yr)
  - PFCs (<100 kgCE/wafer)
    (~25,000 tons CE/yr)

- **Chemicals**
  - Metal / Dielectric precursor chemicals
  - HAPs precursors
  - PFCs precursors
  - Solvents
  - CMP Materials

- **Water**
  - 15.5l/cm² of Si produced
  - ~ a town of 20,000

- **Chips**
  - 100,000 $/kg

- **Solid & liquid waste**
  - Producing 1 PC = 63 kg of waste material generated
    - ~43 kg of non-hazardous waste
    - ~20 kg of hazardous waste

Sources: International Roadmap for Semiconductor, S. Raoux, Applied Materials
**GWP takes into account a molecule’s lifetime and its ability to absorb Infrared radiation**

**PFCs have a high GWP compared to other global warming gases (CO₂, CH₄, N₂O…)**
- PFCs strongly absorb IR radiation: some of the most potent green house gases
- PFCs are chemically very stable: they are hard to destroy and have a long atmospheric lifetime
- Emitting 1 kg of SF₆ is like emitting 6 tons of carbon equivalent or 22.2 tons of CO₂ (100yrs time horizon)

### PFC Emissions Reduction in the semiconductor industry - Drivers -

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<td>Europe</td>
<td>Ratified</td>
<td>Yes</td>
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<td>Yes - Reduce PFC emissions 10% below 1995 baseline</td>
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- **Regulatory and voluntary efforts**
  - UNFCCC / Kyoto Protocol
  - EU and Japanese directives and regulations
  - Regional Memoranda of Understanding (US, EU)
  - World Semiconductor Council voluntary commitment

- **Environmental Stewardship and awareness**
  - ISO 14000 and environmental standards
  - Industry, corporate image
  - National policies
  - Global climate change is real!
Green house gases emissions in the US and the semiconductor industry

- Total US green house gases emissions*: 1,816 MMTCE
- PFC emissions from semiconductor fabrication represents only 0.07% of US green house gas emissions.

Emissions reduction for PFC's proposed by the World Semiconductor Council (WSC) Environmental Safety and Health (ESH) Task Force has been approved by members of the WSC (the European Electronic Component Manufacturers Association or EECA, the Electronic Industries Association of Japan or EIAJ, the Korea Semiconductor Industry Association or KSIA and the Semiconductor Industry Association in the U.S. or SIA) at the third WSC meeting in Fiuggi, Italy on April 23, 1999. The WSC is committed to proactively seek to reduce the emissions of PFC's from their semiconductor manufacturing processes.

PFC emissions from semiconductor manufacturing operations in the US and California

- **US and California emissions estimates using IPCC Tier 1 method**

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<tr>
<td>No. Fabs</td>
<td>%</td>
<td>Area, MSI</td>
<td>%</td>
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<td>75</td>
<td>1.6%</td>
<td>185.96</td>
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<td>0.4%</td>
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<td>6381</td>
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<td>22%</td>
<td>17%</td>
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<td>20%</td>
<td>11%</td>
<td>19%</td>
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</table>

US PFC, US EPA, MMTCE (voluntary control): 1.74
US PFC, PEVM, MMTCE (uncontrolled): 2.30

- **PFC emissions from semiconductor manufacturing in California have decreased from ~0.4-0.5 MMTCE in 2000 to ~0.3-0.4 MMTCE in 2006**

- **US share of world manufacturing capacity has dropped over 2000 - 2006 period, from roughly 25 to 20 percent on an MSI-layer basis.**

- **Note: uncontrolled emissions are emissions that would have occurred under a business-as-usual scenario.**

Source: World Fab Watch, IPCC Tier 1 estimation by Shep Burton and SIA estimates provided by Chuck Fraust
Strategies to Reduce PFC Emissions from Semiconductor manufacturing

Hierarchy *

1 - Change chemistry / byproducts
2 - Improve process efficiency, use better PFCs
3 – Capture PFCs, purify and reuse
4 - Convert / destroy PFCs

PFC Replacement
C₄F₆, C₅F₈, unsaturated FCs, iodo-fluorocarbons
(selected applications only)

PFC abatement
(Plasma, Thermocatalytic, Combustion)

Remote NF₃ Clean
(98% DRE)

In-situ Clean optimization
optimized C₂F₆, NF₃, C₃F₈, c-C₄F₈, C₄F₈O

PFC Abatement
In-situ chamber clean – Combustion / Wet

Modeling Consumption and Emissions on a Per Chip Basis

- Gas consumption and emissions were measured for over 75 processes
- GWGs, HAPs, and VOCs emissions were quantified on a per wafer pass basis
- A model of consumption and emissions can be built for the whole chip

Gas Consumption Per Module:

- Interconnect modules: 47%
- Via modules: 41%
- Gate module: 5%
- Shallow trench isolation module: 7%

Fab growth and PFC emissions reduction goals

1995 Emissions (baseline year) 0.67 MMTCE

2010 Emissions (8% Growth - no action taken) 2.11 MMTCE
- 71.6%

2010 Emissions (15% Growth - no action taken) 5.41 MMTCE
- 88.9%

2010 Emissions Target (10% below baseline year) 0.59 MMTCE

70 to 90% Absolute PFC emissions reduction will be required to meet the 2010 target

Solutions for CVD Chamber Cleaning Optimization

- **Baseline**: Un-optimized C\textsubscript{2}F\textsubscript{6} in-situ clean process (1 mm USG TEOS thin films)
- **Action P1**: Implementation of NF\textsubscript{3} remote clean
- **Action P2**: Implementation of c-C\textsubscript{4}F\textsubscript{8} chemistry for in-situ clean
- **Action P3**: Implementation of C\textsubscript{3}F\textsubscript{8} chemistry for in-situ clean

Solutions for CVD Chamber Cleaning Optimization

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- **Action P3**: Implementation of C$_3$F$_8$ chemistry for in-situ clean

*Includes additional hardware cost depreciated over 5 years, process gases, chamber consumables and abatement costs.*
PFC Abatement Methods

Chemical reactions for PFCs (simplified):

\[ C_x F_y + \text{Oxygen} + \text{Hydrogen} \rightarrow CO, CO_2, COF_2, HF, F_2 \]

- **Reaction temperatures:**
  - Combustion: 300-1200°C
  - Catalytic: 300-700°C
  - Plasma: 150-200°C

- **Combustion**
  - Most suited for high flow applications (when fuel acceptable)
  - CVD in-situ clean, FPD (can be used for Etch)

- **Thermal Catalytic**
  - Most suited for medium flow Etch applications (no fuel)

- **Plasma**
  - Most suited for low flow Etch applications (no fuel, energy efficiency, low footprint)
  - May require post pump (HF) treatment

- **Additional combinations (unproven)**
  - Plasma + oxidation + wet
  - Oxidation + wet + catalytic + wet

Source: S. Raoux, Applied Materials
Reducing Global Warming Emissions Through PFC Emissions Reduction and Lower Energy Consumption

- **Sources and relative impact of solutions to reduce global warming emissions** (in Carbon Equivalent)

<table>
<thead>
<tr>
<th>Year</th>
<th>CVD</th>
<th>Etch</th>
<th>Tool Electrical</th>
<th>Fab Electrical</th>
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<tr>
<td>1995/98</td>
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<td></td>
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<tr>
<td>2010</td>
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1995-98 Baseline ~ 32 kgCE per wafer pass
- CVD cleans ~ 20 kgCE/wp
- Etch ~ 4 kgCE/wp
- Tool electrical consumption ~ 3.2 kgCE
- Fab support electrical consumption ~ 4.8

2000 ~ 15 kgCE per wafer pass
- NF₃ Remote Clean
- Optimized CF₄ / C₂F₆ in-situ clean

2005 ~ 9 kgCE per wafer pass
- NF₃ Remote Clean
- Alternative C₃F₈ / c-C₄F₈ / C₄F₈O in-situ clean
- Etch Abatement
- Efficient pumps

2010 ~ 7 kgCE per wafer pass
- NF₃ Remote Clean
- Alternative C₃F₈ / c-C₄F₈ / C₄F₈O in-situ clean
- Etch abatement
- Efficient pumps
- Efficient fab support equipment

Source: S. Raoux, Applied Materials
Upcoming PFC emissions challenges in California
Other silicon-based manufacturing processes

- Photovoltaic (PV) manufacturing, Micro Electro-Mechanical Systems (MEMS) and Flat Panel Display (FPD) production all use similar processes and chemistries as semiconductor manufacturing does, including the use of PFCs for chamber cleaning and etching.

- The lessons learned in the semiconductor industry must be applied to PV, MEMS and FPD manufacturing.

- While MEMS and FPD manufacturing does not seem to represent a large source of PFC emissions in California, the upcoming development of the solar industry could lead to an increase in PFC emissions.
Photovoltaic shipment and exports (US)

- **California photovoltaic (2005):**
  - Shipment: 55,847 peak kW
  - Exports: 31,952 peak kW

- **Issues:**
  - The DOE report on photovoltaic manufacturing activities is not designed to collect production data, just shipments.
  - What is produced in one year might not be shipped until the next. Sometime these shipments also included imports.
  - An estimation of PFC emissions from solar manufacturing operation in California (and elsewhere) does not seem to exist

- **An estimation of PFC emissions from photovoltaic manufacturing should be considered**

Conclusion

- The latest generation of semiconductor manufacturing tools and processes provide reduced environmental impact and lower cost of ownership
  - PFC emissions can be reduced through process optimization and use of alternative chemistries
  - Further PFC emissions reduction can be obtained through abatement
  - Electrical consumption reduction from semiconductor manufacturing operations will also lead to additional CO₂ emission reductions
  - Integration and interfacing of manufacturing equipment (process tools, pumps, heat exchanger, chillers, RF generators…) will lead to better reliability and reduced environmental impact

- The voluntary WSC commitment seems definitely on a track to succeed
  - But high-growth regions with booming semiconductor production (Korea, Taiwan, Singapore, China) still have difficult problems to solve

- Design for the Environment (DfE) must consider:
  - **Cost of ownership**
    - Capital cost
    - Treatment cost
    - Operation cost
  - **Process performance**
    - Process repeatability
    - Tool productivity
    - Utilization / abatement efficiency
  - **ESH impact**
    - Human health impact
    - Environmental impact
    - Regulatory compliance

Solutions that improve productivity are win-win propositions for the industry and the environment
Acknowledgment

I wish to thank Shep Burton, Chuck Fraust and Peter Wong for research assistance.

THANK YOU FOR YOUR ATTENTION!