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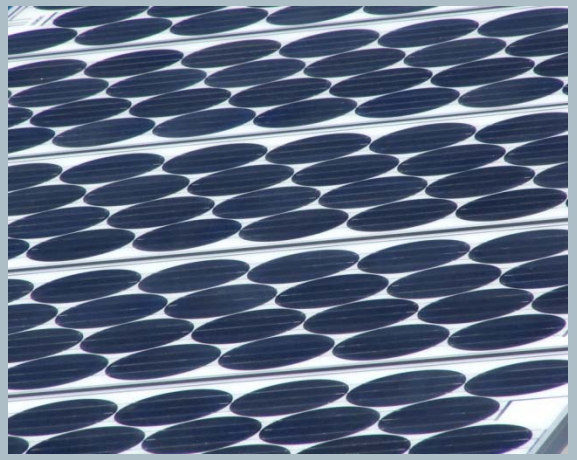


Perfluorocompounds Emissions Reduction in the Semiconductor and Silicon Industries

Sébastien Raoux, Ph.D.

President and CEO
TRANSCARBON INTERNATIONAL

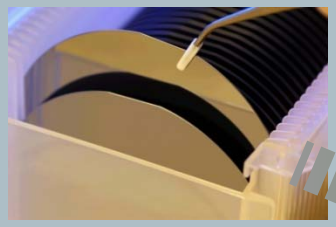
International Symposium on Near-Term Solutions for Climate Change Mitigation in California

March 5-7, 2007
Cal/EPA Headquarters 1001 I Street, Sacramento

The environmental impact of a typical semiconductor Fab

(30,000 wafer starts / month)

- **Si wafers**
  - 10 tons/yr

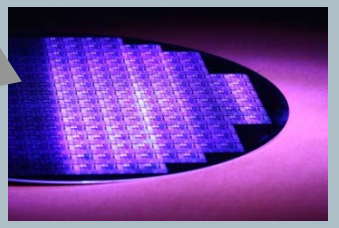


- **Electricity**
  - 0.9kWh/cm^2 of Si produced
  - ~ a town of 7,500.

- **Air emissions**
  - HAPs (max 20 tons/yr)
  - VOCs (max 40-100 tons/yr)
  - PFCs (<100 kgCE/wafer) (~25,000 tons CE/yr)

- **Chemicals**
  - Metal / Dielectric precursor chemicals
  - HAPs precursors
  - PFCs precursors
  - Solvents
  - CMP Materials

- **Chips**
  - 100,000 $/kg



- **Solid & liquid waste**
  - Producing 1 PC = 63 kg of waste material generated
    - ~43 kg of non-hazardous waste
    - ~20 kg of hazardous waste

- **Water**
  - 15.5l/cm^2 of Si produced
  - ~ a town of 20,000

Sources: International Roadmap for Semiconductor, S. Raoux, Applied Materials

PerFluoroCompounds (PFCs), Global Warning Potential (GWP) Carbon and CO_2 Equivalents

	Gas	Atmospheric Lifetime (years)	Global Warming Potential (Time horizon in years)		
			GWP - 100 yrs	GWP - 500 yrs	GWP (infinite)
	CO_2	50-100	1	1	1
Perfluorocompounds	CF_4	50,000	5,700	8,900	850,000
	C_2F_6	10,000	11,900	18,000	230,000
	SF_6	3,200	22,200	32,400	230,000
	C_3F_8	2,600	8,600	12,400	130,000
	NF_3	740	10,970	13,240	18,000
	CHF_3	260	12,000	10,000	11,000
	c-C_4F_8	3,200	10,000	14,500	N/A

$$kgCE = Q(kg)\frac{C^*}{CO_2^*}GWP$$

$$kgCO_2E = Q(kg) \times GWP$$

C*/CO2* = molecular weight ratio
=12/44

- **GWP takes into account a molecule's lifetime and its ability to absorb Infrared radiation**
- **PFCs have a high GWP compared to other global warming gases** (CO_2, CH_4, N_2O…)
  - PFCs strongly absorb IR radiation: some of the most potent green house gases
  - PFCs are chemically very stable: they are hard to destroy and have a long atmospheric lifetime
  - Emitting 1 kg of SF_6 is like emitting 6 tons of carbon equivalent or 22.2 tons of CO_2 (100yrs time horizon)

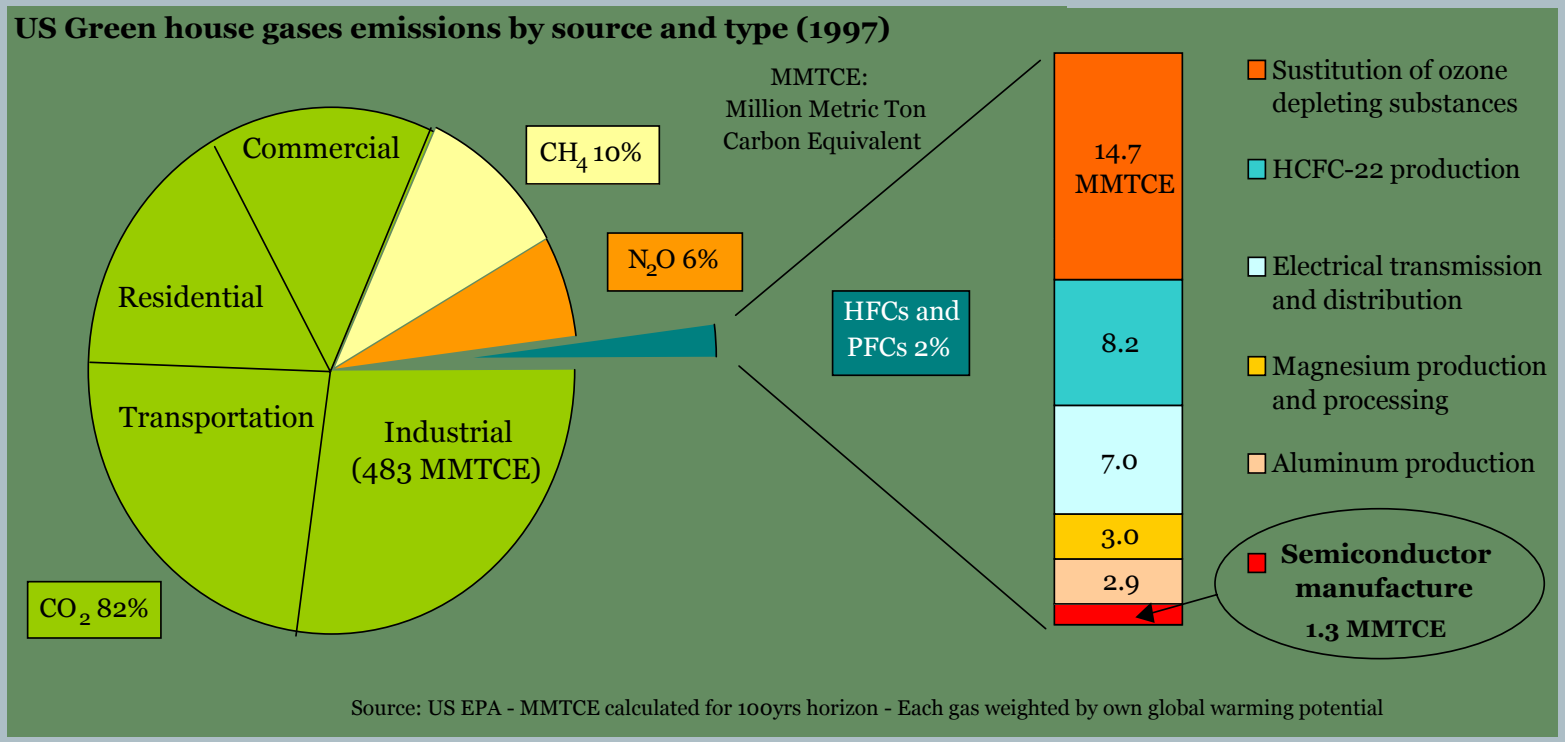
Source: IPCC Third Assessment Report - (Cambridge, UK: Cambridge University Press, 2001); World Meteorological Organization; Report No. 47 (2002)

PFC Emissions Reduction in the semiconductor industry
- Drivers -

PFC Emissions in the Semiconductor Industry	United Nations Framework Convention on Climate Change (UNFCCC)	Kyoto Protocol to the UNFCCC ratified?	Legally binding emission targets under Kyoto?	Regional PFC regulatory requirement in effect?	World Semiconductor Council commitment towards 2010?
Europe	Ratified	Yes	Yes	Yes (European directive 2004/101/EC)	Yes - Reduce PFC emissions 10% below 1995 baseline
Japan	Ratified	Yes	Yes	Yes (some prefectures)	Yes - Reduce PFC emissions 10% below 1995 baseline
Korea	Ratified	Yes	No	No	Yes - Reduce PFC emissions 10% below 1997 baseline
United States	Ratified	No	No	Some states	Yes - Reduce PFC emissions 10% below 1995 baseline
Taiwan	Not a UN Member	Not a UN Member	No	No	Yes - Reduce PFC emissions 10% below 1998 baseline
Singapore	Ratified	Yes	No	No	No
Malaysia	Ratified	Yes	No	No	No
China	Ratified	Yes	No	No	No

- **Regulatory and voluntary efforts**
  - UNFCCC / Kyoto Protocol
  - EU and Japanese directives and regulations
  - Regional Memoranda of Understanding (US, EU)
  - **World Semiconductor Council voluntary commitment**
- **Environmental Stewardship and awareness**
  - ISO 14000 and environmental standards
  - Industry, corporate image
  - National policies
  - Global climate change is real!

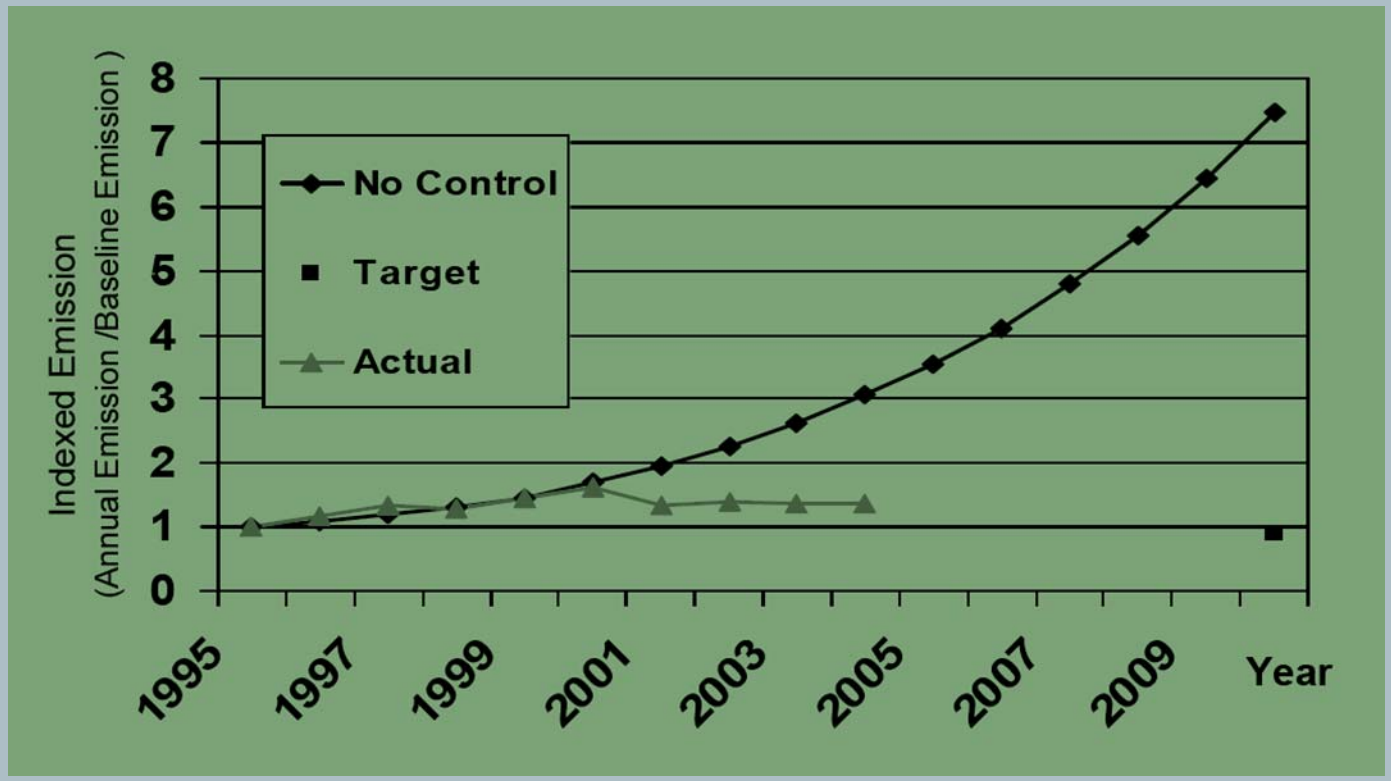
Green house gases emissions in the US and the semiconductor industry



- Total US green house gases emissions*: 1,816 MMTCE
- PFC emissions from semiconductor fabrication represents only 0.07% of US green house gas emissions.

* Source: EPA Report, Inventory of U.S. Greenhouse Gas Emission & Sinks: 1990 - 1996

World Semiconductor Council Voluntary Commitment



- Emissions reduction for PFC's proposed by the World Semiconductor Council (WSC) Environmental Safety and Health (ESH) Task Force has been approved by members of the WSC (the European Electronic Component Manufacturers Association or EECA, the Electronic Industries Association of Japan or EIAJ, the Korea Semiconductor Industry Association or KSIA and the Semiconductor Industry Association in the U.S. or SIA) at the third WSC meeting in Fiuggi, Italy on April 23, 1999. The WSC is committed to proactively seek to reduce the emissions of PFC's from their semiconductor manufacturing processes.

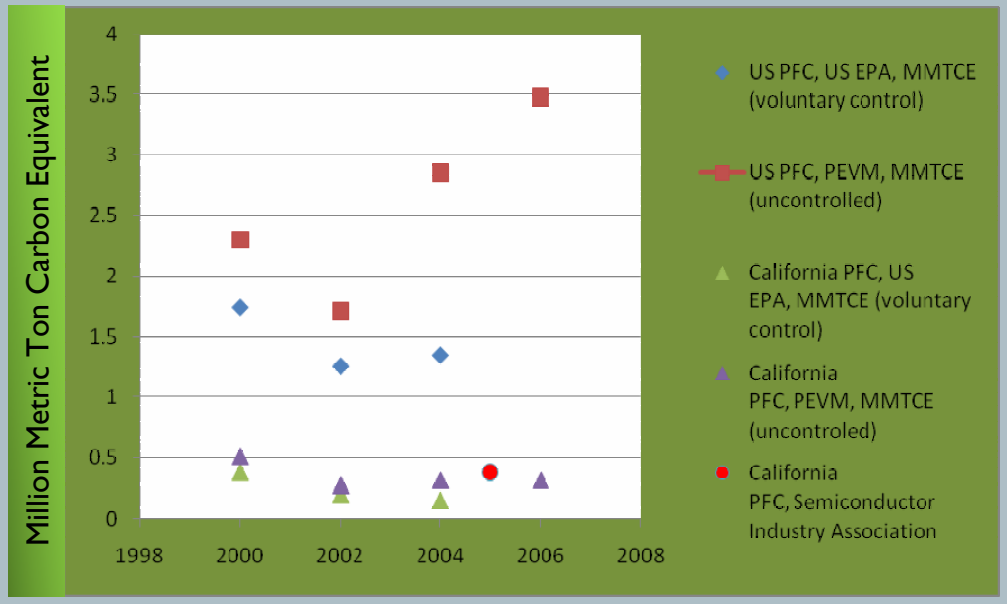
Source: World Semiconductor Council - http://www.semiconductorcouncil.org/news

PFC emissions from semiconductor manufacturing operations in the US and California

- US and California emissions estimates using IPCC Tier 1 method

	2000					2002					2004					2006				
	No. Fabs	Missing Records, %	Area, MSI	MSI-layers	Avg. layers	No. Fabs	Missing Records, %	Area, MSI	MSI-layers	Avg. layers	No. Fabs	Missing Records, %	Area, MSI	MSI-layers	Avg. layers	No. Fabs	Missing Records, %	Area, MSI	MSI-layers	Avg. layers
CA	75	1.6%	185.96	758.27	4.08	55	1.8%	167.45	758.09	4.53	52	1.9%	172.18	709.89	4.12	51	1.6%	140.54	599.98	4.27
US	339	0.4%	NA	3424	NA	322	0.4%	NA	4772	NA	256	0.5%	NA	6381	NA	267	0.4%	1211.80	6897.89	5.69
CA, %US	22%			22%		17%			16%		20%			11%		19%		12%	9%	
US PFC, US EPA, MMTCE (voluntary control):					1.74				1.26					1.35					NA	
US PFC, PEVM, MMTCE (uncontrolled):					2.30				1.71					2.86					3.48	

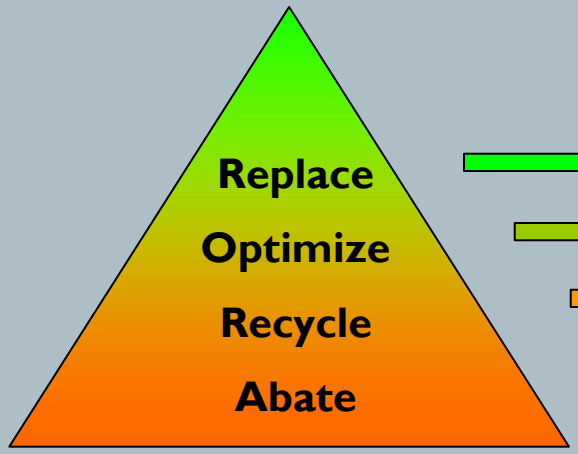
- PFC emissions from semiconductor manufacturing in California have decreased from ~0.4-0.5MMTCE in 2000 to ~0.3-0.4 MMTCE in 2006
- US share of world manufacturing capacity has dropped over 2000 - 2006 period, from roughly 25 to 20 percent on an MSI-layer basis.
- Note: uncontrolled emissions are emissions that would have occurred under a business-as-usual scenario



Source: World Fab Watch, IPCC Tier 1 estimation by Shep Burton and SIA estimates provided by Chuck Fraust

Strategies to Reduce PFC Emissions from Semiconductor manufacturing

Hierarchy *

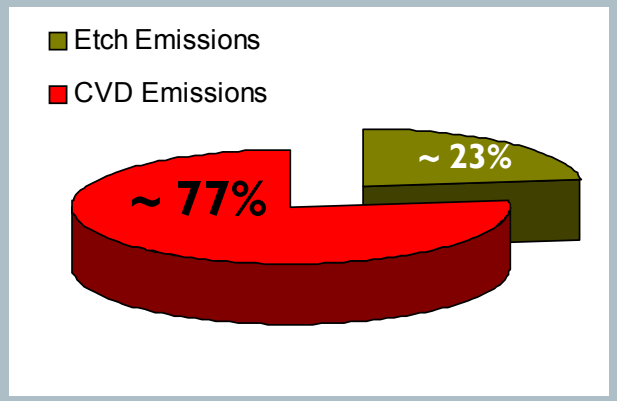


1- Change chemistry / byproducts

2 - Improve process efficiency, use better PFCs

3 – Capture PFCs, purify and reuse

4 - Convert / destroy PFCs



Etch

PFC Replacement
C_4F_6 , C_5F_8, unsaturated FCs, iodo-fluorocarbons
(selected applications only)

PFC abatement
(Plasma, Thermocatalytic, Combustion)

CVD

Remote NF_3 Clean
(98% DRE)

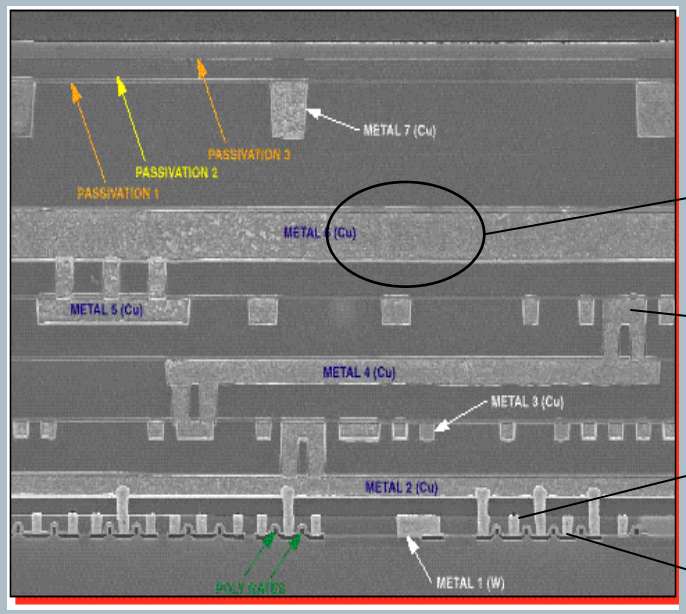
In-situ Clean optimization
optimized C_2F_6; NF_3 C_3F_8; c-C_4F_8; C_4F_8O

PFC Abatement
In-situ chamber clean – Combustion / Wet

* L. Beu et al. *Twenty Third IEEE/CPMT International Electronics Manufacturing Technology Symposium*, 1998, p 277-85

Modeling Consumption and Emissions on a Per Chip Basis

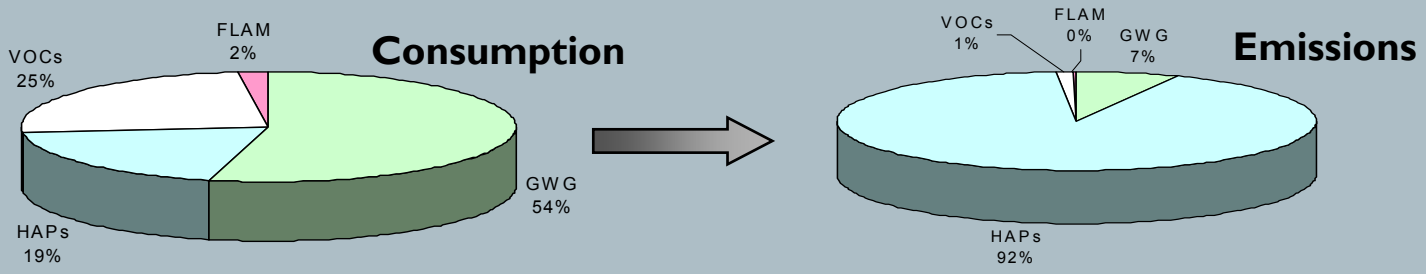
- Gas consumption and emissions were measured for over 75 processes
- GWGs, HAPs, and VOCs emissions were quantified on a per wafer pass basis
- A model of consumption and emissions can be built for the whole chip



Cross section of a logic device with 7 levels of metal

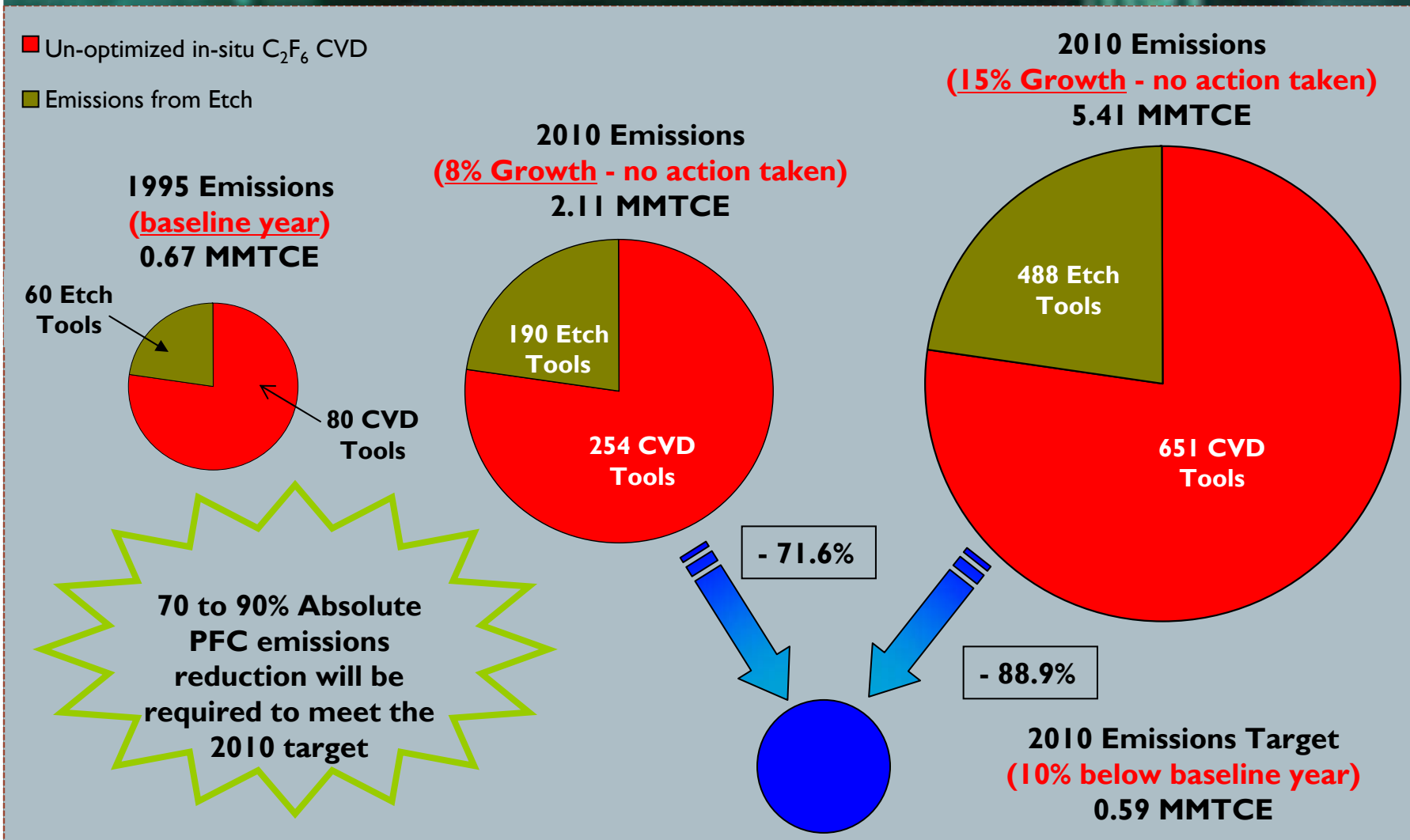
Gas Consumption Per Module:

- Interconnect modules: 47%
- Via modules: 41%
- Gate module: 5%
- Shallow trench isolation module: 7%



Source: Applied Materials. Smati, R., Raoux, S., Ho, D., Woolston, M., "Measuring and modeling gas consumption and emissions from semiconductor manufacturing processes," EHS Assessment Techniques, SEMICON West, 2002.

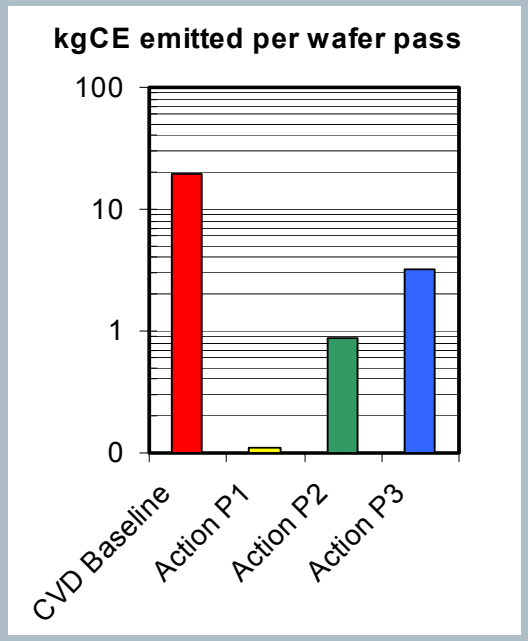
Fab growth and PFC emissions reduction goals

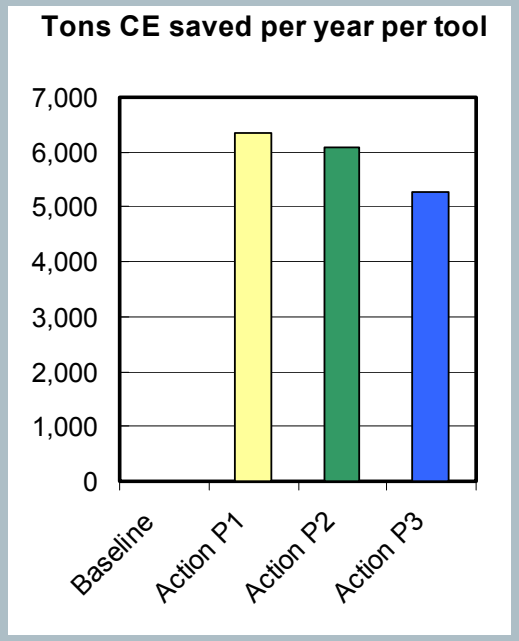


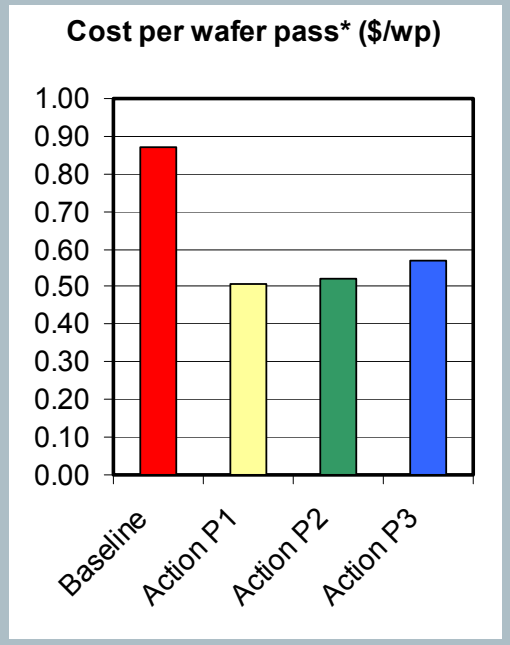
Source: S. Raoux, Applied Materials - *Solid State Technology* - Implementing technologies for reducing PFC emissions – Jan. 2007

Solutions for CVD Chamber Cleaning Optimization

- **Baseline** Un-optimized C_2F_6 in-situ clean process (1mm USG TEOS thin films)
- **Action P1** Implementation of NF_3 remote clean
- **Action P2** Implementation of c-C_4F_8 chemistry for in-situ clean
- **Action P3** Implementation of C_3F_8 chemistry for in-situ clean







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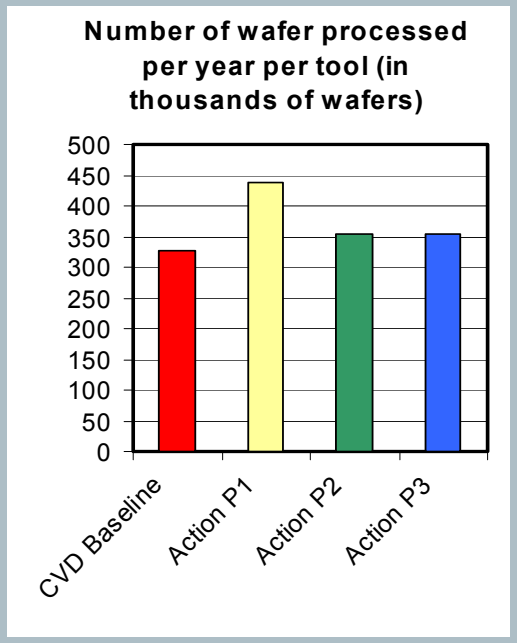
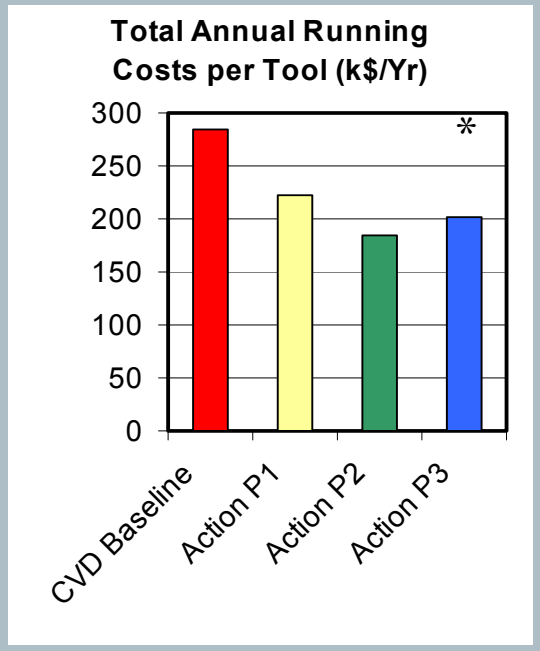
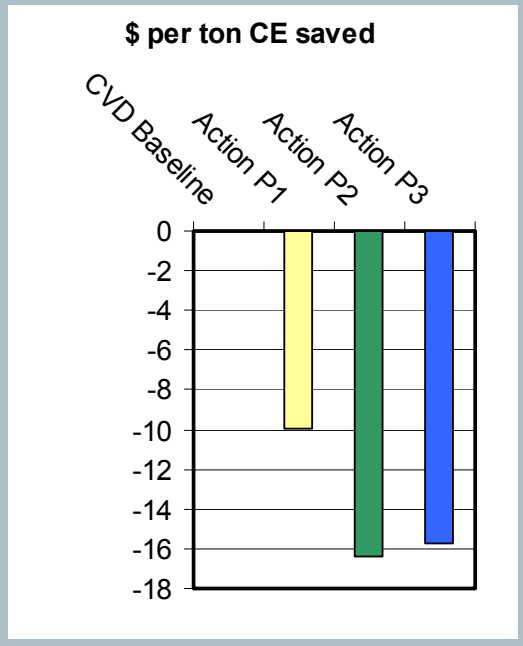






Source: S. Raoux, Applied Materials - *Solid State Technology* - Implementing technologies for reducing PFC emissions – Jan. 2007

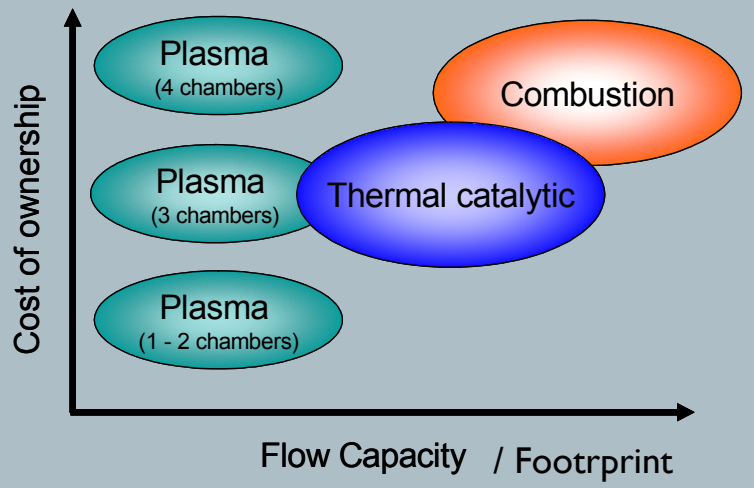
* Includes additional hardware cost depreciated over 5 years, process gases, chamber consumables and abatement costs.

PFC Abatement Methods

Chemical reactions for PFCs (simplified):

$$C_xF_y + Oxygen + Hydrogen \xrightarrow[\text{Combustion}]{\text{Plasma, Catalyst}} CO, CO_2, COF_2, HF, F_2$$

- **Reaction temperatures:**
  - Combustion: 300-1200C
  - Catalytic: 300-700C
  - Plasma: 150-200C
- **Combustion**
  - Most suited for high flow applications (when fuel acceptable)
  - CVD in-situ clean, FPD (can be used for Etch)
- **Thermal Catalytic**
  - Most suited for medium flow Etch applications (no fuel)
- **Plasma**
  - Most suited for low flow Etch applications (no fuel, energy efficiency, low footprint)
  - May require post pump (HF) treatment



- **Additional combinations (unproven)**
  - Plasma + oxidation + wet
  - Oxidation + wet + catalytic + wet

Source: S. Raoux, Applied Materials

Reducing Global Warming Emissions Through PFC Emissions Reduction and Lower Energy Consumption

- **Sources and relative impact of solutions to reduce global warming emissions (in Carbon Equivalent)**

1995/98 → 2000 → 2005 → 2010

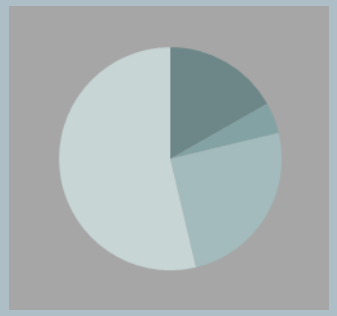
CVD Etch Tool Electrical Fab Electrical

1995-98 Baseline ~ 32 kgCE per wafer pass

- CVD cleans ~ 20 kgCE/wp
- Etch ~ 4 kgCE/wp
- Tool electrical consumption ~ 3.2 kgCE
- Fab support electrical consumption ~ 4.8

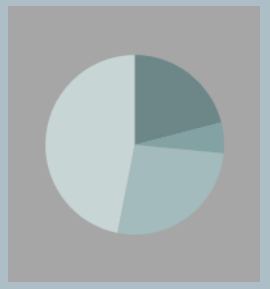
2000 ~ 15 kgCE per wafer pass

- **NF_3 Remote Clean**
- Optimized CF_4 / C_2F_6 in-situ clean



2005 ~ 9 kgCE per wafer pass

- NF_3 Remote Clean
- **Altenative C_3F_8 c-C_4F_8 , C_4F_8O… in-situ clean**
- **Etch Abatement**
- **Efficient pumps**



2010 ~ 7 kgCE per wafer pass

- NF_3 Remote Clean
- Altenatice C_3F_8 / c-C_4F_8 C_4F_8O… in-situ clean
- Etch abatement
- Efficient pumps
- **Efficient fab support equipment**

Source: S. Raoux, Applied Materials

Upcoming PFC emissions challenges in California
Other silicon-based manufacturing processes

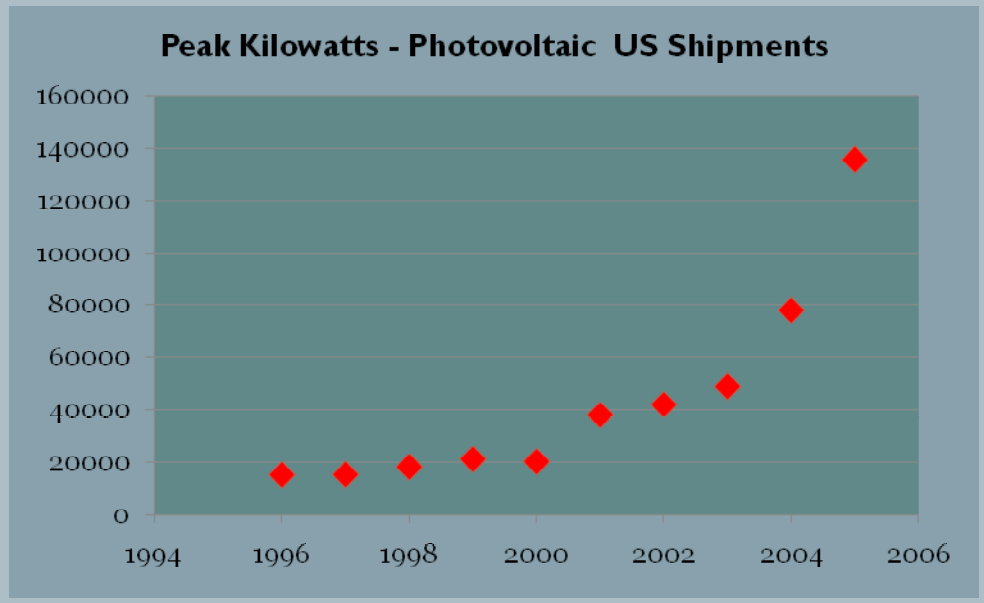
- **Photovoltaic (PV)** manufacturing, **Micro Electro-Mechanical Systems (MEMS)** and **Flat Panel Display (FPD)** production all use similar processes and chemistries as semiconductor manufacturing does, including the use of PFCs for chamber cleaning and etching.

Courtesy Sandia National Laboratories
SUMMiT™ Technologies
www.mems.sandia.gov

- The lessons learned in the semiconductor industry must be applied to PV, MEMS and FPD manufacturing.
- While MEMS and FPD manufacturing does not seem to represent a large source of PFC emissions in California, the upcoming development of the solar industry could lead to an increase in PFC emissions.

Photovoltaic shipment and exports (US)

- **California photovoltaic (2005):**
  - Shipment: 55,847 peak kW
  - Exports: 31,952 peak kW
- **Issues:**
  - The DOE report on photovoltaic manufacturing activities is not designed to collect production data, just shipments .
  - What is produced in one year might not be shipped until the next. Sometime these shipments also included imports.
  - An estimation of PFC emissions from solar manufacturing operation in California (and elsewhere) does not seem to exist
- **An estimation of PFC emissions from photovoltaic manufacturing should be considered**



Source: Solar Thermal and Photovoltaic Collector Manufacturing Activities 2005. Energy Information Administration.

Conclusion

- **The latest generation of semiconductor manufacturing tools and processes provide reduced environmental impact and lower cost of ownership**
  - PFC emissions can be reduced through process optimization and use of alternative chemistries
  - Further PFC emissions reduction can be obtained through abatement
  - Electrical consumption reduction from semiconductor manufacturing operations will also lead to additional CO_2 emission reductions
  - Integration and interfacing of manufacturing equipment (process tools, pumps, heat exchanger, chillers, RF generators…) will lead to better reliability and reduced environmental impact
- **The voluntary WSC commitment seems definitely on a track to succeed**
  - But high-growth regions with booming semiconductor production (Korea, Taiwan, Singapore , China) still have difficult problems to solve
- **Design for the Environment (DfE) must consider:**
  - **Cost of ownership**
    - Capital cost
    - Treatment cost
    - Operation cost
  - **Process performance**
    - Process repeatability
    - Tool productivity
    - Utilization / abatement efficiency
  - **ESH impact**
    - Human health impact
    - Environmental impact
    - Regulatory compliance

Solutions that improve productivity are win-win propositions for the industry and the environment

Ackowledgment

I wish to thank Shep Burton, Chuck Fraust and Peter Wong for research assistance.

THANK YOU FOR YOUR ATTENTION!